Stability in Weak Memory Models
Table of Power assembly instructions

Jade Alglave[1,2] and Luc Maranget[2]

[1] University of Oxford [2] INRIA

Name	Code	Comment
plain load	`lwz r1,0,r2`	loads into `r1` from the address in `r2`
plain store	`stw r1,0,r2`	stores from `r1` into the address in `r2`
load reserve	`lwarx r1,0,r2`	loads from the address in `r2` into `r1` and reserves the address in `r2`
store conditional	`stwcx. r1,0,r2`	checks if the address in `r2` is reserved; if so, stores from `r1` into this address; if not, fails
branch not equal	`bne L`	checks if a certain register holds 0, if not branches to `L`
compare	`cmpw r4, r6`	compares values in `r4` and `r6`
isync	`isync`	when placed after a `bne`, forms a RW, RR non-cumulative barrier
lwsync	`lwsync`	RW, RR, WW A- and B-cumulative barrier
sync	`sync`	RW, RR, WW, WR A- and B-cumulative barrier