1002
Logic gates and Transistors

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Materials

Metals - an electron is released by each metal atom to form electron 'soup'.
Applying an electric field across metal moves electron soup: a current flows.

Insulators - atoms in insulators keep all their electrons firmly attached.
No electron 'soup' is created,
and no current will flow in response to an applied electric field.

Semiconductors: these are normally weakly conducting when pure,
conduction can be increased by 'doping': adding other materials.

Silicon doped with phosphorus atoms produces an n-type material:
n-types semiconductors: electrons carry current.

Silicon doped with boron atoms produces a p-type material:
p-type semiconductors: 'holes' carry current.
Silicon Diode:

Allows current flow in only one direction!

Electrons can be made to flow from n-type to p-type: 
this will only happen if p-type region is more positive than n-type.

It is very difficult to make electrons and holes flow the other way.
Electrons can move from n-type to p-type but not from p-type to n-type. Thus would not expect current to flow from source to drain or drain to source. Current will flow if can make n-type region (the channel) between source/drain.

Symbols for an n-transistor:

- substrate is ~1000 microns deep / n-type diffusions are 0.2-1 microns deep / (1 millimetre = 1000 microns)

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METAL-OXIDE-SILICON (MOS)  n-p-n transistor.

Channel is created if gate is at 5V:
electric field pulls electrons into the region next to the insulator, making channel region n-type. Current can now flow between source/drain - 'switch' closed.

When the gate is at 0V, there is no electric field across insulator to hold extra electrons in the Channel region and the Channel dissappears:
current can no longer flow - channel region is now p-type - 'switch' open.
Operation of n-p-n transistor (n-channel or n-transistor)

1. Offstate of device with Gate at 0V. No electrons flow between left n-region into substrate across p-n junction, because both sides of junction are at 0V.

No electrons flow between right n-region and substrate because p-n junction is reversed biased:
- voltage on n-region is either same or greater than substrate - a voltage lower than substrate is needed on n-region to get electrons out of it into p-region.

2. When Gate is put to 5V, the electric field effectively puts 5V on the substrate below the gate. This voltage pulls electrons from the left n-region to create a n-type channel. (channel is partially formed in this diagram)
Operation of n-p-n transistor (n-channel or n-transistor)

3.

Eventually (~500ps) the n-type channel reaches the right n-region, and the electrons in the channel screen the substrate from the electric field. The voltage in the channel is 0V. At this stage, electrons can flow through the channel.

4.

When the gate is put back to 0V, the n-channel with its excess electrons appears to be at less than 0V (due to excess negative charge), and the greater voltage (0V) on the n-regions and substrate attracts the electrons and the channel disappears.
Electrons can move from n-type to p-type but not from p-type to n-type. Thus would not expect current to flow from source to drain or drain to source.

Current will flow if can make p-type region (the channel) between source/drain.

Symbols for an n-transistor :-

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<table>
<thead>
<tr>
<th>gate</th>
<th>drain</th>
<th>gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>source</td>
<td></td>
<td>source</td>
</tr>
</tbody>
</table>
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substrate is ~1000 microns deep / n-type diffusions are 0.2-1 microns deep/ (1 millimetre = 1000 microns)
METAL-OXIDE-SILICON (MOS)  p-n-p transistor.

Channel is created if gate is at 0V:
electric field pulls holes into the region next to the insulator, making channel region p-type. Current can now flow between source/drain - 'switch' closed.

When the gate is at 5V, there is no electric field across insulator to hold extra electrons in the Channel region and the Channel dissappears:
current can no longer flow - channel region is now n-type - 'switch' open.
Operation of p-n-p transistor (p-channel or p-transistor)

Offstate of device with Gate at 5V.
No electrons flow into left p-region from substrate across p-n junction because both sides of junction are at 5V.

No electrons flow between right p-region and substrate because p-n junction is reversed biased:
voltage on p-region is either same or less than substrate: a voltage greater than substrate is needed on the p-region to get electrons to flow into it.

When Gate is put to 0V, the electric field effectively puts 0V on the substrate below the gate. This voltage allows holes from the left p-region to create a p-type channel, i.e. electrons are pulled out of the channel into the left p-region. (channel is partially formed in this diagram)
Operation of p-n-p transistor (p-channel or p-transistor)

Eventually (~500ps) the p-type channel reaches the right p-region, and the lack of electrons in the channel screens the substrate from the electric field. The voltage in the channel is 5V.

At this stage, any voltage on the right p-region lower than 5V will pull holes through the channel from the left p-region, i.e. electrons to flow in the opposite direction.

When the gate is put back to 5V, instantaneously the p-channel with its lack of electrons appears to be at greater than 5V (due to excess positive charge), and this will attract electrons from the p-regions and substrate and the channel disappears.
**NMOS Logic**

This consists of only n-transistors (n-p-n):
- Transistor conducts when gate is at 5V
- Transistors is not-conducting when gate is at 0V

Inverters, nand and nor gates can be made in the same way as our electronic switch circuits except that, since simple resistors take up very large areas, special weakly-conducting transistors are used.

These have the same function as resistors of limiting the current flow when the circuit outputs a '0'.

![NMOS Inverter Diagram]

While lower transistor is conducting, current flows and power consumed. It takes longer to go from '0' to '1' than from '1' to '0', because better conductivity from 0V to output than from 5V to output.

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2-INPUT NAND

3-INPUT NOR

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CMOS Logic - Complimentary MOS

Uses both n-p-n and p-n-p transistors

Inverter

Either upper p transistor is conduction or lower n-type, but not both: 'complimentary' operation

When input is 5V, is there is path from 0V through n-transistor to output

When input is 0V, there is a path from 5v through p-transistor to output

In steady state, output is connected either to 0V or to 5V by conducting transistors, but not to both. This is complimentary action.
There is never a good conducting path from 5V to 0V, i.e. A short-circuit condition never exists.
There is also no steady-state current through the transistors.
CMOS Logic - Complimentary MOS

Inverter

Uses both n-p-n and p-n-p transistors

Either upper p transistor is conduction or lower n-type, but not both: 'complimentary' operation

As circuit switches, electrons move first from 0V supply to gate output and second from gate output to 5V supply – on each output cycle (0 --> 1 --> a bunch of electrons move from 0V to 5V and power is consumed from the power supply

Therefore power consumed only when circuit switching: low power circuits, power increases with operating frequency.

CMOS switches output very fast in both directions, because good conducting paths to 0V and 5V.
2-Input NOR gate in CMOS

Bottom section of circuit generates zero outputs

Top section of circuit generates 5V outputs

'Switch' Model with $A = B = 0V$

These 2 equations are the same by deMorgan's

Top section generates 1s in truth table; bottom section generates 0s
2-input NAND

Only when both A & B are 5V, is there path through n-types to output

When either A or B is 0V, there is a path to 5V but no path to 0V.
2-INPUT OR circuit from 2-INPUT NOR and INVERTOR

Switch' representation for A = B = 5V

Note: There is no conducting pathway between the NOR circuit and the transistors of the INVERTOR along the output line C. C affects the operation of the transistors of the INVERTOR by means of the electric field of the voltage on C across the gate insulator: no continuous current flows along C along C at any time.
CMOS Logic - Complimentary MOS

CMOS uses both type of transistor (n-p-n) and (p-n-p) on same substrate.

How? By building an n-type well in p-type substrate.

- n-p-n in p-substrate conducts when at 5V
- p-n-p in 'in-well' conducts when at 0V
- reversed biased p-n junction
Liquid P-type Silicon

Large single crystal grown

Cut to cylinder shape.....

... and sliced into wafers

5 or 8 inch diameter wafers
Surface of p-type wafer

Surface exposed to oxygen - Silicon Oxide Layer forms on surface

Surface coated with photo-sensitive material

Surface is covered by a photographic mask and exposed to light
Surface is etched with acid exposing surface where special layer has been exposed to light.

Oven filled with Phosphorus vapour

Phosphorus atoms shoot out of oven and bombard surface

Phosphorus atoms enter substrate only where surface exposed: they bounce off oxide layer

2 n-type regions produced in p-type material
Surface exposed to oxygen again to get silicon oxide layer

Polysilicon layer deposited over surface

Surface is coated with photo-sensitive material, covered by a photographic mask and exposed to light

Surface is etched away to oxide surface where sensitised by light.

Transistor produced

...and repeat adding metal layers, connectors between layers....
MAGNACHIP SEMICONDUCTOR STARTS PRODUCTION

THE NON-MEMORY unit of Hynix Semiconductor began operations in Korea last month under the new name of MagnaChip Semiconductor.

Huh Youm, reckons that the company, with its extensive research capabilities, could become one of the world’s largest producers of semiconductors. “Our independent