x86-64 Programming I: Introduction

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UCL Computer Science

CS 3007
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(lecture notes derived from material from Phil Gibbons, Randy Bryant, and Dave O’Hallaron)
Today: x86-64 Basics

- History of Intel processors and architectures
- Assembly Basics: Registers, operands, move
- Arithmetic & logical operations
- C, assembly, machine code
Intel x86 Processors

- Dominate laptop/desktop/server market

- Evolutionary design
  - Backwards compatible up until 8086, introduced in 1978
  - Added more features as time goes on

- Complex instruction set computer (CISC)
  - Many different instructions with many different formats
    - But, only small subset encountered with Linux programs
  - Hard to match performance of Reduced Instruction Set Computers (RISC)
  - But, Intel has done just that!
    - In terms of speed. Less so for low power.
## Intel x86 Evolution: Milestones

<table>
<thead>
<tr>
<th>Name</th>
<th>Date</th>
<th>Transistors</th>
<th>MHz</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>8086</td>
<td>1978</td>
<td>29K</td>
<td>5-10</td>
<td>First 16-bit Intel processor, Basis for IBM PC &amp; DOS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1MB address space</td>
</tr>
<tr>
<td>386</td>
<td>1985</td>
<td>275K</td>
<td>16-33</td>
<td>First 32 bit Intel processor, referred to as IA32</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Added “flat addressing”, capable of running Unix</td>
</tr>
<tr>
<td>Pentium 4E</td>
<td>2004</td>
<td>125M</td>
<td>2800-3800</td>
<td>First 64-bit Intel x86 processor, referred to as x86-64</td>
</tr>
<tr>
<td>Core 2</td>
<td>2006</td>
<td>291M</td>
<td>1060-3333</td>
<td>First multi-core Intel processor</td>
</tr>
<tr>
<td>Core i7</td>
<td>2008</td>
<td>731M</td>
<td>1600-4400</td>
<td>Four cores</td>
</tr>
</tbody>
</table>
Intel x86 Processors, cont.

■ Machine Evolution

- 386 1985 0.3M
- Pentium 1993 3.1M
- Pentium/MMX 1997 4.5M
- PentiumPro 1995 6.5M
- Pentium III 1999 8.2M
- Pentium 4 2000 42M
- Core 2 Duo 2006 291M
- Core i7 2008 731M

■ Added Features

- Instructions to support multimedia operations
- Instructions to enable more efficient conditional operations
- Transition from 32 bits to 64 bits
- More cores
## Intel x86 Processors, cont.

### Past Generations

<table>
<thead>
<tr>
<th>Generation</th>
<th>Year</th>
<th>Process Technology</th>
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</thead>
<tbody>
<tr>
<td>1st Pentium Pro</td>
<td>1995</td>
<td>600 nm</td>
</tr>
<tr>
<td>1st Pentium III</td>
<td>1999</td>
<td>250 nm</td>
</tr>
<tr>
<td>1st Pentium 4</td>
<td>2000</td>
<td>180 nm</td>
</tr>
<tr>
<td>1st Core 2 Duo</td>
<td>2006</td>
<td>65 nm</td>
</tr>
</tbody>
</table>

### Recent & Upcoming Generations

1. Nehalem 2008 45 nm
2. Sandy Bridge 2011 32 nm
3. Ivy Bridge 2012 22 nm
4. Haswell 2013 22 nm
5. Broadwell 2014 14 nm
6. Skylake 2015 14 nm
7. Kaby Lake 2016 14 nm
8. Coffee Lake 2017? 14 nm
9. Cannonlake 2018? 10 nm

Process technology dimension = width of narrowest wires
(10 nm ≈ 100 atoms wide)
2017 State of the Art: Skylake

- **Mobile Model: Core i7**
  - 2.6-2.9 GHz
  - 45 W

- **Desktop Model: Core i7**
  - Integrated graphics
  - 2.8-4.0 GHz
  - 35-91 W

- **Server Model: Xeon**
  - Integrated graphics
  - Multi-socket enabled
  - 2-3.7 GHz
  - 25-80 W
x86 Clones: Advanced Micro Devices (AMD)

- Historically
  - AMD has followed just behind Intel
  - A little bit slower, a lot cheaper

- Then
  - Recruited top circuit designers from Digital Equipment Corp. and other downward trending companies
  - Built Opteron: tough competitor to Pentium 4
  - Developed x86-64, their own extension to 64 bits

- Recent Years
  - Intel got its act together
    - Leads the world in semiconductor technology
  - AMD has fallen behind
    - Relies on external semiconductor manufacturer
Intel’s 64-Bit History

- **2001: Intel Attempts Radical Shift from IA32 to IA64**
  - Totally different architecture (Itanium)
  - Executes IA32 code only as legacy
  - Performance disappointing

- **2003: AMD Steps in with Evolutionary Solution**
  - x86-64 (now called “AMD64”)

- **Intel Felt Obligated to Focus on IA64**
  - Hard to admit mistake or that AMD is better

- **2004: Intel Announces EM64T extension to IA32**
  - Extended Memory 64-bit Technology
  - Almost identical to x86-64!

- **All but low-end x86 processors support x86-64**
  - But, lots of code still runs in 32-bit mode
Intel Architecture Variants

- IA32
  - The traditional, 32-bit x86

- x86-64
  - The standard
    - `shark> gcc hello.c`
    - `shark> gcc -m64 hello.c`

- Presentation
  - Book covers x86-64
  - Web aside on IA32
  - We will only cover x86-64
Today: Machine Programming I: Basics

- History of Intel processors and architectures
- Assembly Basics: Registers, operands, move
- Arithmetic & logical operations
- C, assembly, machine code
Levels of Abstraction

C programmer

C code

Assembly programmer

Computer Designer

Caches, clock freq, layout, ...
Levels of Abstraction

C programmer

Assembly programmer

CPU

PC

Registers

Condition Codes

Addresses

Data

Instructions

Memory

Code

Data

Stack

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Caches, clock freq, layout, ...
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Nice, clean layers, but beware…
Levels of Abstraction

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Nice, clean layers, but beware...

Of course, you know that: It’s why you are taking this class.
Definitions

- **Architecture**: (also ISA: instruction set architecture)
  The parts of a processor design that one needs to understand for writing correct machine/assembly code
  - Examples: instruction set specification, registers
  - **Machine Code**: The byte-level programs that a processor executes
  - **Assembly Code**: A text representation of machine code

- **Microarchitecture**: Implementation of the architecture
  - Examples: cache sizes and core frequency

- **Example ISAs**:
  - Intel: x86, IA32, Itanium, x86-64
  - ARM: Used in almost all mobile phones
  - RISC V: New open-source ISA
Assembly/Machine Code View

Programmer-Visible State

- **PC: Program counter**
  - Address of next instruction
  - Called “RIP” (x86-64)

- **Register file**
  - Heavily used program data

- **Condition codes**
  - Store status information about most recent arithmetic or logical operation
  - Used for conditional branching

**Memory**

- Byte addressable array
- Code and user data
- Stack to support procedures
Assembly Characteristics: Data Types

- “Integer” data of 1, 2, 4, or 8 bytes
  - Data values
  - Addresses (untyped pointers)

- Floating point data of 4, 8, or 10 bytes

- (SIMD vector data types of 8, 16, 32 or 64 bytes)

- Code: Byte sequences encoding series of instructions

- No aggregate types such as arrays or structures
  - Just contiguously allocated bytes in memory
## x86-64 Integer Registers

<table>
<thead>
<tr>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>%rax</td>
</tr>
<tr>
<td>%rbx</td>
</tr>
<tr>
<td>%rcx</td>
</tr>
<tr>
<td>%rdx</td>
</tr>
<tr>
<td>%rsi</td>
</tr>
<tr>
<td>%rdi</td>
</tr>
<tr>
<td>%rsp</td>
</tr>
<tr>
<td>%rbp</td>
</tr>
<tr>
<td>%eax</td>
</tr>
<tr>
<td>%ebx</td>
</tr>
<tr>
<td>%ecx</td>
</tr>
<tr>
<td>%edx</td>
</tr>
<tr>
<td>%esi</td>
</tr>
<tr>
<td>%edi</td>
</tr>
<tr>
<td>%esp</td>
</tr>
<tr>
<td>%ebp</td>
</tr>
<tr>
<td>%r8</td>
</tr>
<tr>
<td>%r9</td>
</tr>
<tr>
<td>%r10</td>
</tr>
<tr>
<td>%r11</td>
</tr>
<tr>
<td>%r12</td>
</tr>
<tr>
<td>%r13</td>
</tr>
<tr>
<td>%r14</td>
</tr>
<tr>
<td>%r15</td>
</tr>
</tbody>
</table>

- Can reference low-order 4 bytes (also low-order 1 & 2 bytes)
- Not part of memory (or cache)
Some History: IA32 Registers

- %eax
- %ecx
- %edx
- %ebx
- %esi
- %edi
- %esp
- %ebp
Some History: IA32 Registers

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<th>AX Registers</th>
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<td>%eax</td>
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</tr>
<tr>
<td>%ecx</td>
<td>%cx</td>
</tr>
<tr>
<td>%edx</td>
<td>%dx</td>
</tr>
<tr>
<td>%ebx</td>
<td>%bx</td>
</tr>
<tr>
<td>%esi</td>
<td>%si</td>
</tr>
<tr>
<td>%edi</td>
<td>%di</td>
</tr>
<tr>
<td>%esp</td>
<td>%sp</td>
</tr>
<tr>
<td>%ebp</td>
<td>%bp</td>
</tr>
</tbody>
</table>

%al, %dl, %bl are 8-bit registers.
Some History: IA32 Registers

16-bit virtual registers (backwards compatibility)
Some History: IA32 Registers

- **%eax** (%ax: %ah, %al)
- **%ecx** (%cx: %ch, %cl)
- **%edx** (%dx: %dh, %dl)
- **%ebx** (%bx: %bh, %bl)
- **%esi** (%si)
- **%edi** (%di)
- **%esp** (%sp)
- **%ebp** (%bp)

**Origin (mostly obsolete)**
- Accumulate
- Counter
- Data
- Base
- Source
- Index
- Destination
- Index
- Stack
- Pointer
- Base
- Pointer

16-bit virtual registers (backwards compatibility)
Assembly Characteristics: Operations

- Transfer data between memory and register
  - Load data from memory into register
  - Store register data into memory

- Perform arithmetic function on register or memory data

- Transfer control
  - Unconditional jumps to/from procedures
  - Conditional branches
  - Indirect branches
Moving Data

Moving Data

movq *Source, Dest*

Operand Types

- **Immediate**: Constant integer data
  - Example: $0x400, $-533
  - Like C constant, but prefixed with ‘$’
  - Encoded with 1, 2, or 4 bytes

- **Register**: One of 16 integer registers
  - Example: %rax, %r13
  - But %rsp reserved for special use
  - Others have special uses for particular instructions

- **Memory**: 8 consecutive bytes of memory at address given by register
  - Simplest example: (%rax)
  - Various other “addressing modes”
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\textbf{Warning: Intel docs use mov Dest, Source}
**movq** **Operand Combinations**

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*Cannot do memory-memory transfer with a single instruction*
**movq** Operand Combinations

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<td></td>
</tr>
<tr>
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<td>Mem</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>Reg, Mem</td>
<td>movq $0x4,%rax temp = 0x4;</td>
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**movq** Operand Combinations

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*Cannot do memory-memory transfer with a single instruction*
Simple Memory Addressing Modes

- Normal (R) Mem[Reg[R]]
  - Register R specifies memory address
  - Aha! Pointer dereferencing in C

  ```
  movq (%rcx), %rax
  ```

- Displacement D(R) Mem[Reg[R]+D]
  - Register R specifies start of memory region
  - Constant displacement D specifies offset

  ```
  movq 8(%rbp), %rdx
  ```
Example of Simple Addressing Modes

void whatAmI(<type> a, <type> b)
{
    ????
}

whatAmI:
    movq (%rdi), %rax
    movq (%rsi), %rdx
    movq %rdx, (%rdi)
    movq %rax, (%rsi)
    ret
Example of Simple Addressing Modes

void whatAmI(<type> a, <type> b)
{
    // ???
}

whatAmI:
    movq (%rdi), %rax
    movq (%rsi), %rdx
    movq %rdx, (%rdi)
    movq %rax, (%rsi)
    ret

%rdi
Example of Simple Addressing Modes

```c
void whatAmI(<type> a, <type> b)
{
    ????
}
```

```assembly
whatAmI:
    movq (%rdi), %rax
    movq (%rsi), %rdx
    movq %rdx, (%rdi)
    movq %rax, (%rsi)
    ret
```
Example of Simple Addressing Modes

```c
void swap
    (long *xp, long *yp)
{
    long t0 = *xp;
    long t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```assembly
swap:
    movq (%rdi), %rax
    movq (%rsi), %rdx
    movq %rdx, (%rdi)
    movq %rax, (%rsi)
    ret
```
Understanding `swap()`

```c
void swap (long *xp, long *yp)
{
    long t0 = *xp;
    long t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

**Registers**

- `%rdi`: `xp`
- `%rsi`: `yp`
- `%rax`: `t0`
- `%rdx`: `t1`

**Swap:**

```
movq (%rdi), %rax  # t0 = *xp
movq (%rsi), %rdx  # t1 = *yp
movq %rdx, (%rdi)  # *xp = t1
movq %rax, (%rsi)  # *yp = t0
ret
```
Understanding `Swap()`

### Registers

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`swap:`

```
movq    (%rdi), %rax  # t0 = *xp
movq    (%rsi), %rdx  # t1 = *yp
movq    %rdx, (%rdi)  # *xp = t1
movq    %rax, (%rsi)  # *yp = t0
ret
```
Understanding \texttt{Swap()}

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### Memory

- Address: 0x120
- 123: 0x120
- 456: 0x110
- 0x118
- 0x108
- 0x100

#### swap:

- \texttt{movq (\%rdi), \%rax}  \# t0 = *xp
- \texttt{movq (\%rsi), \%rdx}  \# t1 = *yp
- \texttt{movq \%rdx, (\%rdi)}  \# *xp = t1
- \texttt{movq \%rax, (\%rsi)}  \# *yp = t0
- \texttt{ret}
Understanding `swap()`

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**swap:**

```assembly
movq (%rdi), %rax  # t0 = *xp
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movq %rdx, (%rdi)  # *xp = t1
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```
### Understanding `Swap()`

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#### `swap:`

- `movq (%rdi), %rax` # `t0 = *xp`
- `movq (%rsi), %rdx` # `t1 = *yp`
- `movq %rdx, (%rdi)` # `*xp = t1`
- `movq %rax, (%rsi)` # `*yp = t0`
- `ret`
Understanding `Swap()`

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### Code

```assembly
swap:
    movq (%rdi), %rax       # t0 = *xp
    movq (%rsi), %rdx       # t1 = *yp
    movq %rdx, (%rdi)       # *xp = t1
    movq %rax, (%rsi)       # *yp = t0
    ret
```
Simple Memory Addressing Modes

- Normal (R) \(\text{Mem}[\text{Reg}[R]]\)
  - Register R specifies memory address
  - Aha! Pointer dereferencing in C

  \[
  \text{movq } (\%rcx),\%rax
  \]

- Displacement D(R) \(\text{Mem}[\text{Reg}[R]+D]\)
  - Register R specifies start of memory region
  - Constant displacement D specifies offset

  \[
  \text{movq } 8(\%rbp),\%rdx
  \]
Complete Memory Addressing Modes

- **Most General Form**
  
  \[ D(Rb, Ri, S) \quad \text{Mem}[\text{Reg}[Rb] + S*\text{Reg}[Ri] + D] \]
  
  - **D:** Constant “displacement” 1, 2, or 4 bytes
  - **Rb:** Base register: Any of 16 integer registers
  - **Ri:** Index register: Any, except for \%rsp
  - **S:** Scale: 1, 2, 4, or 8 (*why these numbers?*)

- **Special Cases**
  
  \[
  \begin{align*}
  \text{(Rb, Ri)} & \quad \text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri]] \\
  \text{D(Rb, Ri)} & \quad \text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] + D] \\
  \text{(Rb, Ri, S)} & \quad \text{Mem}[\text{Reg}[Rb] + S*\text{Reg}[Ri]]
  \end{align*}
  \]
## Address Computation Examples

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## D(Rb,Ri,S) \ Mem[Reg[Rb]+S*Reg[Ri]+ D]

- **D**: Constant “displacement” 1, 2, or 4 bytes
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D(Rb,Ri,S) Mem[Reg[Rb]+S*Reg[Ri]+ D]

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**D(Rb,Ri,S) = Mem[Reg[Rb]+S*Reg[Ri]+ D]**

- **D:** Constant “displacement” 1, 2, or 4 bytes
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**D(Rb,Ri,S)**  
**Mem[Reg[Rb]+S*Reg[Ri]+ D]**

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\[D(\text{Rb, Ri, S}) = \text{Mem[Reg[Rb]+S*Reg[Ri]} + D\]

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Today: Machine Programming I: Basics

- History of Intel processors and architectures
- Assembly Basics: Registers, operands, move
- Arithmetic & logical operations
- C, assembly, machine code
Address Computation Instruction

- **leaq** *Src, Dst*
  - *Src* is address mode expression
  - Set *Dst* to address denoted by expression

- **Uses**
  - Computing addresses without a memory reference
    - E.g., translation of `p = &x[i];`
  - Computing arithmetic expressions of the form `x + k*y`
    - `k = 1, 2, 4, or 8`

- **Example**

```c
long m12(long x)
{
    return x*12;
}
```

**Converted to ASM by compiler:**

```asm
leaq (%rdi,%rdi,2), %rax  # t = x+2*x
salq $2, %rax             # return t<<2
```
## Some Arithmetic Operations

- **Two Operand Instructions:**

<table>
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<tr>
<td>addq</td>
<td>Dest = Dest + Src</td>
</tr>
<tr>
<td>subq</td>
<td>Dest = Dest – Src</td>
</tr>
<tr>
<td>imulq</td>
<td>Dest = Dest * Src</td>
</tr>
<tr>
<td>salq</td>
<td>Dest = Dest &lt;&lt; Src</td>
</tr>
<tr>
<td>sarq</td>
<td>Dest = Dest &gt;&gt; Src</td>
</tr>
<tr>
<td>shrq</td>
<td>Dest = Dest &gt;&gt;&gt; Src</td>
</tr>
<tr>
<td>xorq</td>
<td>Dest = Dest ^ Src</td>
</tr>
<tr>
<td>andq</td>
<td>Dest = Dest &amp; Src</td>
</tr>
<tr>
<td>orq</td>
<td>Dest = Dest</td>
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- Watch out for argument order! *Src, Dest*  
  (Warning: Intel docs use “op *Dest, Src*)
- No distinction between signed and unsigned int (why?)
Some Arithmetic Operations

- **One Operand Instructions**
  - `incq` \( Dest \) \( Dest = Dest + 1 \)
  - `decq` \( Dest \) \( Dest = Dest - 1 \)
  - `negq` \( Dest \) \( Dest = -Dest \)
  - `notq` \( Dest \) \( Dest = \sim Dest \)

- See CS:APP/3e for more instructions
Arithmetic Expression Example

```
long arith
(long x, long y, long z)
{
    long t1 = x+y;
    long t2 = z+t1;
    long t3 = x+4;
    long t4 = y * 48;
    long t5 = t3 + t4;
    long rval = t2 * t5;
    return rval;
}
```

Interesting Instructions

- **leaq**: address computation
- **salq**: shift
- **imulq**: multiplication
  - But, only used once
Understanding Arithmetic Expression Example

```c
long arith
(long x, long y, long z)
{
    long t1 = x+y;
    long t2 = z+t1;
    long t3 = x+4;
    long t4 = y * 48;
    long t5 = t3 + t4;
    long rval = t2 * t5;
    return rval;
}
```

```
arith:
    leaq (%rdi,%rsi), %rax    # t1
    addq %rdx, %rax           # t2
    leaq (%rsi,%rsi,2), %rdx
    salq $4, %rdx             # t4
    leaq 4(%rdi,%rdx), %rcx  # t5
    imulq %rcx, %rax          # rval
    ret
```

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<thead>
<tr>
<th>Register</th>
<th>Use(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>%rdi</td>
<td>Argument x</td>
</tr>
<tr>
<td>%rsi</td>
<td>Argument y</td>
</tr>
<tr>
<td>%rdx</td>
<td>Argument z, t4</td>
</tr>
<tr>
<td>%rax</td>
<td>t1, t2, rval</td>
</tr>
<tr>
<td>%rcx</td>
<td>t5</td>
</tr>
</tbody>
</table>
Today: Machine Programming I: Basics

- History of Intel processors and architectures
- Assembly Basics: Registers, operands, move
- Arithmetic & logical operations
- C, assembly, machine code
Turning C into Object Code

- Code in files `p1.c p2.c`
- Compile with command: `gcc -Og p1.c p2.c -o p`
  - Use basic optimizations (`-Og`) [New to recent versions of GCC]
  - Put resulting binary in file `p`

```
C program (p1.c p2.c)
```

```
Compiler (gcc -Og -S)
```

```
Asm program (p1.s p2.s)
```

```
Assembler (gcc or as)
```

```
Object program (p1.o p2.o)
```

```
Linker (gcc or ld)
```

```
Executable program (p)
```

Static libraries (.a)
### Compiling Into Assembly

#### C Code (sum.c)

```c
long plus(long x, long y);

void sumstore(long x, long y, long *dest) {
    long t = plus(x, y);
    *dest = t;
}
```

#### Generated x86-64 Assembly

```
sumstore:
    pushq  %rbx
    movq  %rdx, %rbx
    call  plus
    movq  %rax, (%rbx)
    popq  %rbx
    ret
```

Obtain with command

```
gcc -Og -S sum.c
```

Produces file `sum.s`

Warning: Will yield different results on different machines (Linux, Mac OS-X, ...) because of different gcc versions (or other compilers, like LLVM/clang) and different compiler settings.
What it really looks like

```
.globl sumstore
.type sumstore, @function

sumstore:
.LFB35:
  .cfi_startproc
  pushq %rbx
  .cfi_def_cfa_offset 16
  .cfi_offset 3, -16
  movq %rdx, %rbx
  call plus
  movq %rax, (%rbx)
  popq %rbx
  .cfi_def_cfa_offset 8
  ret
  .cfi_endproc
.LFE35:
  .size sumstore, .-sumstore
```
What it really looks like

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.globl sumstore
.type sumstore, @function
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.LFB35:
    .cfi_startproc
    pushq  %rbx
    .cfi_def_cfa_offset 16
    .cfi_offset 3, -16
    movq   %rdx, %rbx
    call   plus
    movq   %rax, (%rbx)
    popq   %rbx
    .cfi_def_cfa_offset 8
    ret
    .cfi_endproc
.LFE35:
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```assembly
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  movq  %rax, (%rbx)
  popq  %rbx
  .cfi_def_cfa_offset 8
  ret
  .cfi_endproc

.LFE35:
  .size  sumstore, -.sumstore
```
Object Code

Code for `sumstore`

0x0400595:
- 0x53
- 0x48
- 0x89
- 0xd3
- 0xe8
- 0xf2
- 0xffff
- 0xffff
- 0x48
- 0x89
- 0x03
- 0xc3
- Total of 14 bytes
- Each instruction 1, 3, or 5 bytes
- Starts at address 0x0400595

- **Assembler**
  - Translates `.s` into `.o`
  - Binary encoding of each instruction
  - Nearly-complete image of executable code
  - Missing linkages between code in different files

- **Linker**
  - Resolves references between files
  - Combines with static run-time libraries
    - E.g., code for `malloc, printf`
  - Some libraries are *dynamically linked*
    - Linking occurs when program begins execution
Machine Instruction Example

**C Code**
- Store value \( t \) where designated by \( \text{dest} \)

**Assembly**
- Move 8-byte value to memory
  - Quad words in x86-64 parlance
- Operands:
  - \( t: \) Register \( \%rax \)
  - \( \text{dest}: \) Register \( \%rbx \)
  - \( \ast \text{dest}: \) Memory \( M[\%rbx] \)

**Object Code**
- 3-byte instruction
- Stored at address \( 0x40059e \)
## Disassembling Object Code

### Disassembled

<table>
<thead>
<tr>
<th>Address</th>
<th>Instruction</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000000000400595</td>
<td><code>push %rbx</code></td>
<td></td>
</tr>
<tr>
<td>400595: 53</td>
<td>push %rbx</td>
<td></td>
</tr>
<tr>
<td>400596: 48 89 d3</td>
<td>mov %rdx, %rbx</td>
<td></td>
</tr>
<tr>
<td>400599: e8 f2 ff ff ff</td>
<td>callq 400590 &lt;plus&gt;</td>
<td></td>
</tr>
<tr>
<td>40059e: 48 89 03</td>
<td>mov %rax, (%rbx)</td>
<td></td>
</tr>
<tr>
<td>4005a1: 5b</td>
<td>pop %rbx</td>
<td></td>
</tr>
<tr>
<td>4005a2: c3</td>
<td>retq</td>
<td></td>
</tr>
</tbody>
</table>

### Disassembler

```bash
objdump -d sum
```

- Useful tool for examining object code
- Analyzes bit pattern of series of instructions
- Produces approximate rendition of assembly code
- Can be run on either `a.out` (complete executable) or `.o` file
Alternate Disassembly

Disassembled

Dump of assembler code for function sumstore:
0x000000000000400595 <+0>: push %rbx
0x000000000000400596 <+1>: mov %rdx,%rbx
0x000000000000400599 <+4>: callq 0x400590 <plus>
0x00000000000040059e <+9>: mov %rax,(%rbx)
0x0000000000004005a1 <+12>: pop %rbx
0x0000000000004005a2 <+13>: retq

Within gdb Debugger
  - Disassemble procedure
gdb sum
disassemble sumstore
Alternate Disassembly

Disassembled

Object

0x400595:

0x53
0x48
0x89
0xdd3
0xe8
0xf2
0xff
0xff
0xff
0x48
0x89
0x03
0x5b
0xc3

Dump of assembler code for function sumstore:

0x0000000000400595 <+0>: push %rbx
0x0000000000400596 <+1>: mov %rdx, %rbx
0x0000000000400599 <+4>: callq 0x400590 <plus>
0x000000000040059e <+9>: mov %rax, (%rbx)
0x00000000004005a1 <+12>: pop %rbx
0x00000000004005a2 <+13>: retq

■ Within gdb Debugger

- Disassemble procedure
  
  gdb sum
disable sumstore
- Examine the 14 bytes starting at sumstore
  x/14xb sumstore
What Can be Disassembled?

- Anything that can be interpreted as executable code
- Disassembler examines bytes and reconstructs assembly source

% objdump -d WINWORD.EXE

WINWORD.EXE: file format pei-i386

No symbols in "WINWORD.EXE".
Disassembly of section .text:

30001000 <.text>:
30001000:
30001001:
30001003:
30001005:
3000100a:

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x86-64 Programming I: Summary

- History of Intel processors and architectures
  - Evolutionary design leads to many quirks and artifacts
- C, assembly, machine code
  - New forms of visible state: program counter, registers, ...
  - Compiler must transform statements, expressions, procedures into low-level instruction sequences
- Assembly Basics: Registers, operands, move
  - The x86-64 move instructions cover wide range of data movement forms
- Arithmetic
  - C compiler will figure out different instruction combinations to carry out computation